RECEIVED
CENTRAL FAX CENTER
JUL 18 2005

Fax transmission from:

U.S. Naval Research Laboratory
Associate Counsel Intellectual Property, Code 1008.2
4555 Overlook Avenue, SW
Washington, DC 20375-5325

From: Joe Grunkemeyer
Phone: (202) 404-1556
Fax: (202) 404-7380

To: Examiner Kenneth S. Kim
Art Unit 2111
Fax: (571) 273-8300

Date: 07/18/2005

Cover Sheet + 15 Pages

Message:

RE: Patent Application No.: 09/933,786
Filed: 08/20/2001
Inventor: Sandbote
Docket No.: NC 84,832
Appeal Brief Transmittal – 2 pages
Appeal Brief – 10 pages
Fee Transmittal – 1 page
Copy of facsimile receipt and Notice of Appeal – 2 pages

PATENT APPLICATION
Navy Case No.: 84,832

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of: Sandbote
Serial No.: 09/933,786
Filed: 08/20/2001
For: SHIFT PROCESSING UNIT
Examiner: Kim, Kenneth S.
Art Group Unit: 2111

Honorable Commissioner of Patents
PO Box 1450
Alexandria, VA 22313-1450

July 18, 2005

APPEAL BRIEF TRANSMITTAL

Sir:

Attached is Applicant's Appeal Brief for this appeal and Fee Transmittal. Also attached is a copy of the Notice of Appeal filed by fax on 05/18/2005 and Auto-Reply Facsimile Transmission showing receipt of the Notice by the USPTO. The Notice was filed within the period of extension previously petitioned for on 05/02/2005. The Notice of Appeal is not found in the image file wrapper of the application. The fax cover sheet inadvertently stated the wrong serial number. However, the Notice of Appeal states the correct serial number and should be treated as filed on 05/18/2005. Thus, no further extension fees are required. However, if

07/19/2005 TL0111 00000028 500281 09933786
01 FC:1402 500.00 DA

CERTIFICATE OF FASCMILE TRANSMISSION

I certify that this correspondence is being facsimile transmitted to the US Patent and Trademark Office on the date shown below.

7/18/05
Date

Joseph T. Grunkemeyer

extension fees or any other fee are required, please charge the fee to Deposit Account No. 50-0281, and in the event that there is a credit due, please credit Deposit Account No. 50-0281.

Respectfully submitted,

Joseph T. Grunkemeyer
Reg. No. 46,746
Phone No. 202-404-1556
Office of the Associate Counsel
(Patents), Code 1008.2
Naval Research Laboratory
4555 Overlook Ave, SW
Washington, DC 20375-5325

PATENT APPLICATION
Navy Case No.: 84,832

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of: Sandbote
Serial No.: 09/933,786
Filed: 08/20/2001
For: SHIFT PROCESSING UNIT
Examiner: Kim, Kenneth S.
Art Group Unit: 2111

Honorable Commissioner of Patents
PO Box 1450
Alexandria, VA 22313-1450

July 18, 2005

APPEAL BRIEF

Sir:

The present appeal is taken from the 01/18/2005 final rejection of claims 1-33 (all claims presently under consideration). A copy of the claims on appeal, as amended in the 12/17/2004 Amendment after Non-Final Rejection, is attached as the Appendix.

REAL PARTY IN INTEREST

The real party in interest is the United States Government, as represented by the Secretary of the Navy.

RELATED APPEALS AND INTERFERENCES

Appellant is unaware of any other appeals, interferences, or judicial proceedings that are related to, will directly affect or be directly affected by, or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

All claims (1-33) are presently rejected.

STATUS OF AMENDMENTS

No amendments have been filed after final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 recites an apparatus comprising a shift post processor, a shifter, and a register coupled to the shift post processor and the shifter (0032, Fig. 3). The shifter can shift an operand according to an offset parameter, generating a shifted operand (0033, lines 1-5). The register is capable of transferring a shift carry operand stored in the register to the shift post processor (0035, lines 5-7) and is capable of storing the shifted operand after any transfer of the shift carry operand (0042-0043). The shift post processor is coupled to the shifter and the register to process the shifted operand (0035, lines 1-2) to generate an output (0055) based on at least a control signal (0035, lines 5-8) and a mask field (0054, lines 3-4). The shift post processor comprises a decoder to decode the offset parameter into the mask field having a plurality of mask bits (0054, lines 1-2). Each of the mask bits corresponds to a bit position of the shifted operand (0054, lines 2-3).

Independent claim 21 recites a processing unit including all the limitations of claim 1. This claim further recites a register file (0022, line 1), an instruction decoder (0021; line 1), and a shift processing unit (0023, line 1). The register file has a plurality of registers (0022, line 1). Each of the registers stores an operand (0022, lines 1-2). The instruction decoder decodes an instruction (0021, line 1). The shift processing unit is coupled (Fig. 1) to the register file and the instruction decoder to perform an operation on the operand (0023, line 1). The shift processing unit is the apparatus recited in claim 1.

Independent claim 11 recites a method comprising shifting an operand (0033, line 3), storing the shifted operand (0034, line 1), and processing the shifted operand (0034, lines 1-4). The operand is shifted according to an offset parameter, generating a shifted operand (0033, lines 1-5). The shifted operand is stored in a register capable of transferring a shift carry operand stored in the register before storing the shifted operand (0042-0043). The shifted operand is processed (0035, lines 1-2) to generate an output (0055) based on at least a control signal (0035, lines 5-8) and a mask field (0054, lines 3-4) by a processing method comprising decoding the offset parameter into the mask field, the mask field having a plurality of mask bits (0054, lines 1-2), each of the mask bits corresponding to a bit position of the shifted operand (0054, lines 2-3).

Thus, when a first shift is performed the output is stored in the register and sent to the shift post processor. In the register it is referred to as the shift carry operand. In a second shift, the shift carry operand is sent from the register to the shift post processor, while the output of the

shifter is again stored in the register and sent to the shift post processor. The shift post processor may then use both the present shifted operand and the previous shifted operand (shift carry operand) for its operations.

There are no mean plus function or step plus function limitations in any of the claims.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1, 2, 11, 12, 21, and 22 stand rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Groves, U.S. Patent No. 5,222,225.

B. Claims 3-10, 13-20, 23-30, and 31-33 stand rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Groves, U.S. Patent No. 5,222,225, in view of Prioste, U.S. Patent No. 4,149,263.

ARGUMENT

A. Claims 1, 2, 11, 12, 21, and 22 recite patentable subject matter over Groves.

Groves discloses a method and system of manipulating a contiguous variable length sequence of data (abstract, lines 2-4). The method can manipulate and shift individual bytes within words (col. 2, lines 44-47). The method uses masks having as many bits are there are bytes in a word. Each bit of a mask indicates how a byte should be processed (col. 4, lines 63-68).

In order to make a *prima facie* case of obviousness, the references must disclose each limitation of the claims. *In re Royka*, 180 U.S.P.Q. 580, 582, 490 F.2d 981, 984 (CCPA 1974). Among other deficiencies, the reference does not teach or suggest the limitation in claims 1, 11, and 21 that each of the mask bits corresponds to a bit position of the shifted operand. This mask allows for shifting by any number of bits, from 1 to the length of the word. Groves is directed to the manipulation of text strings where each character occupies an entire byte (col. 2, lines 44-47). Groves teaches shifting only by entire bytes. There is no teaching or suggestion that shifting be done at the bit level. In fact, Groves teaches against this. If text strings were shifted by numbers of bits other than entire bytes, then the bits making up each character would be spread across two bytes. When such shifted text is read byte-by-byte, the correct characters would not be present.

A *prima facie* case of obviousness also requires a suggestion or motivation to modify the reference. *In re Oetiker*, 24 U.S.P.Q.2d 1443, 1446, 977 F.2d 1443, 1447 (Fed. Cir. 1992). The Examiner stated that a person of ordinary skill would be motivated to use a mask corresponding to bit positions when the shift desired is in units of bits instead of bytes (Office Action of 01/18/2005, p. 3, lines 13-15). However, the reference does not show any desire to shift by bits. Groves is directed to "processing character string moves" (title). As explained above, the proposed modification of shifting by individual bits would render the reference unsatisfactory for its intended purpose, thus no such suggestion or motivation may be found in the reference. *In re Gordon*, 221 U.S.P.Q. 1125, 1127, 733 F.2d 900, 902 (Fed. Cir. 1984).

The Examiner cited portions of Groves (col. 1, line 27; col. 2, line 35) referring to bits as the smallest unit (Office Action of 01/18/2005, p. 3, lines 11-13). However, Groves states only that it would be desirable to access nibbles, as opposed to bits. There is no mention of the desirability of shifting by nibbles as a means to access nibbles. There is no mention of the desirability of accessing individual bits or of shifting by bits.

The third element of a *prima facie* case of obviousness is a reasonable expectation of success. *In re Merck & Co., Inc.*, 231 U.S.P.Q. 375, 379, 800 F.2d 1091, 1097 (Fed. Cir. 1986). The Examiner has not put forth any statements regarding this element.

As all of the claim limitations have not been taught or suggested, there is no motivation to modify the reference, and there has been no showing of a reasonable expectation of success, a *prima facie* case of obviousness has not been made.

Claim 2, 12, and 22 depend from and contain all the limitations of claims 1, 11, and 21, respectively, and are asserted to distinguish from the reference at least in the same manner as claims 1, 11, and 21.

B. Claims 3-10, 13-20, 23-30, and 31-33 recite patentable subject mater over the combination of Groves and Prioste.

The rejected claims depend from and contain all the limitations of claims 1, 11, and 21, while reciting additional limitations.

Prioste discloses a multi-bit shifter for numeric data that can shift by individual bits. The Examiner cited this reference as disclosing shifting numeric bit data with sign and zero extension

(p. 4, lines 4-5).

As explained above, the mask field is not disclosed in Groves and it is not stated as disclosed in Prioste.

There is no motivation to combine the references. Groves is directed to character strings and Prioste is directed to numeric data. There would be no need to add sign and zero extension to text. If shifting as in Prioste were applied to the character strings of Groves, the text would be garbled.

The Examiner stated that the person of ordinary skill "would have been motivated to use the digital data processing method to process numeric data, as numeric data is a subset of digital data" (p. 4, lines 8-9). However, the numeric data of Prioste is not a subset of the textual data of Groves.

There is also no finding regarding a reasonable expectation of success. As all of the claim limitations have not been taught or suggested, there is no motivation to modify the references, and there has been no showing of a reasonable expectation of success, a *prima facie* case of obviousness has not been made.

CONCLUSION

For the reasons stated above, reversal of the rejections under 35 U.S.C. § 103 are earnestly solicited.

In the event that a fee is required, please charge the fee to Deposit Account No. 50-0281, and in the event that there is a credit due, please credit Deposit Account No. 50-0281.

Respectfully submitted,

Joseph T. Grunkemeyer
Reg. No. 46,746
Phone No. 202-404-1556
Office of the Associate Counsel
(Patents), Code 1008.2
Naval Research Laboratory
4555 Overlook Ave, SW
Washington, DC 20375-5325

APPENDIX-THE CLAIMS ON APPEAL

1. An apparatus comprising:

a shift post processor;

a shifter to shift an operand according to an offset parameter, generating a shifted operand; and

a register coupled to the shift post processor capable of transferring a shift carry operand stored in the register to the shift post processor, and coupled to the shifter to store the shifted operand after any transfer of the shift carry operand;

wherein the shift post processor is coupled to the shifter and the register to process the shifted operand to generate an output based on at least a control signal and a mask field, and

wherein the shift post processor comprises a decoder to decode the offset parameter into the mask field, the mask field having a plurality of mask bits, each of the mask bits corresponding to a bit position of the shifted operand.

2. The apparatus of claim 1 wherein the shift post processor further comprises:

at least one bit formatter coupled to the decoder to format the shifted operand using the control signal and the mask field.

3. The apparatus of claim 1 wherein the control signal is one of a zero extension signal, a sign extension signal, and a use shift carry signal.

4. The apparatus of claim 3 wherein when the mask bit is negated, the corresponding bit in the shifted operand is passed through unmodified.

5. The apparatus of claim 3 wherein when the mask bit is asserted, the corresponding bit in the shifted operand is operated upon according to the control signal.

6. The apparatus of claim 2 wherein the bit formatter comprises:
a gating circuit to gate the control signal using the mask bit; and
a selector circuit coupled to the gating circuit to select one of a bit at the bit position of the shifted operand, the shift carry operand, and a most significant bit of the operand based on the gated control signal.

7. The apparatus of claim 6 wherein the selector circuit selects the bit at the bit position of the shifted operand when the mask bit is negated.

8. The apparatus of claim 6 wherein the selector circuit selects the bit at the bit position of the shifted operand when the mask bit is asserted, the zero extension signal is asserted, the sign extension signal is negated, and the use shift carry signal is negated.

9. The apparatus of claim 6 wherein the selector circuit selects the bit at the bit position of the shift carry operand when the mask bit is asserted and the use shift carry signal is asserted.

10. The apparatus of claim 6 wherein the selector circuit selects the most significant bit when the mask bit is asserted, the zero extension signal and the use shift carry signal are negated, and the sign extension signal is asserted.

11. A method comprising:
shifting an operand according to an offset parameter, generating a shifted operand;
storing the shifted operand in a register capable of transferring a shift carry operand stored in the register before storing the shifted operand; and
processing the shifted operand to generate an output based on at least a control signal and a mask field by a processing method comprising decoding the offset parameter into the mask field, the mask field having a plurality of mask bits, each of the mask bits corresponding to a bit position of the shifted operand.

12. The method of claim 11 wherein processing the shifted operand further comprises: formatting the shifted operand using the control signal and the mask field.

13. The method of claim 11 wherein the control signal is one of a zero extension signal, a sign extension signal, and a use shift carry signal.

14. The method of claim 13 wherein when the mask bit is negated, the corresponding bit in the shifted operand is passed through unmodified.

15. The method of claim 13 wherein when the mask bit is asserted, the corresponding bit in the shifted operand is operated upon according to the control signal.

16. The method of claim 12 wherein formatting comprises:
gating the control signal using the mask bit; and
selecting one of a bit at the bit position of the shifted operand, the shift carry operand, and a most significant bit of the operand based on the gated control signal.

17. The method of claim 16 wherein selecting comprises selecting the bit at the bit position of the shifted operand when the mask bit is negated.

18. The method of claim 16 wherein selecting comprises selecting the bit at the bit position of the shifted operand when the mask bit is asserted, the zero extension signal is asserted, the sign extension signal is negated, and the use shift carry signal is negated.

19. The method of claim 16 wherein selecting comprises selecting the bit at the bit position of the shift carry operand when the mask bit is asserted and the use shift carry signal is asserted.

20. The method of claim 16 wherein selecting comprises selecting the most significant bit when the mask bit is asserted, the zero extension signal and the use shift carry signal are negated, and the sign extension signal is asserted.

21. A processing unit comprising:
a register file having a plurality of registers, each of the register storing an operand;
an instruction decoder to decode an instruction; and
a shift processing unit coupled to the register file and the instruction decoder to perform an operation on the operand, the shift processing unit comprising:
a shift post processor;
a shifter to shift an operand according to an offset parameter, generating a shifted operand; and
a register coupled to the shift post processor capable of transferring a shift carry operand stored in the register to the shift post processor, and coupled to the shifter to store the shifted operand after any transfer of the shift carry operand;
wherein the shift post processor is coupled to the shifter and the register to process the shifted operand to generate an output based on at least a control signal and a mask field, and
wherein the shift post processor comprises a decoder to decode the offset parameter into the mask field, the mask field having a plurality of mask bits, each of the mask bits corresponding to a bit position of the shifted operand.

22. The processing unit of claim 21 wherein the shift post processor further comprises:
at least one bit formatter coupled to the decoder to format the shifted operand using the control signal and the mask field.

23. The processing unit of claim 21 wherein the control signal is one of a zero extension signal, a sign extension signal, and a use shift carry signal.

24. The processing unit of claim 23 wherein when the mask bit is negated, the corresponding bit in the shifted operand is passed through unmodified.

25. The processing unit of claim 23 wherein when the mask bit is asserted, the corresponding bit in the shifted operand is operated upon according to the control signal.

26. The processing unit of claim 22 wherein the bit formatter comprises:
a gating circuit to gate the control signal using the mask bit; and
a selector circuit coupled to the gating circuit to select one of a bit at the bit position of the shifted operand, the shift carry operand, and a most significant bit of the operand based on the gated control signal.

27. The processing unit of claim 26 wherein the selector circuit selects the bit at the bit position of the shifted operand when the mask bit is negated.

28. The processing unit of claim 26 wherein the selector circuit selects the bit at the bit position of the shifted operand when the mask bit is asserted, the zero extension signal is asserted, the sign extension signal is negated, and the use shift carry signal is negated.

29. The processing unit of claim 26 wherein the selector circuit selects the bit at the bit position of the shift carry operand when the mask bit is asserted and the use shift carry signal is asserted.

30. The processing unit of claim 26 wherein the selector circuit selects the most significant bit when the mask bit is asserted, the zero extension signal and the use shift carry signal are negated, and the sign extension signal is asserted.

31. The apparatus of claim 3, wherein the use shift carry signal instructs the shift post processor to process the shifted operand based on the shift carry operand.

32. The method of claim 13, wherein, in response to the use shift carry signal, the processing step is based on a shift carry operand transferred from the register before the shifted operand is stored in the register.

33. The processing unit of claim 23, wherein the use shift carry signal instructs the shift post processor to process the shifted operand based on the shift carry operand.

PATENT APPLICATION
Navy Case No.: 84,832

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of: Sandbote
Serial No.: 09/933,786
Filed: 08/20/2001
For: SHIFT PROCESSING UNIT
Examiner: Kim, Kenneth S.
Art Group Unit: 2111

Honorable Commissioner of Patents
PO Box 1450
Alexandria, VA 22313-1450

July 18, 2005

FEE TRANSMITTAL

Sir:

Please charge the Appeal Brief fee under 37 C.F.R. 1.42.20(b)(2) of $500 to Deposit Account No. 50-0281.

In the event that an additional fee is required, please charge the fee to Deposit Account No. 50-0281, and in the event that there is a credit due, please credit Deposit Account No. 50-0281.

Respectfully submitted,

Joseph T. Grunkemeyer
Reg. No. 46,746
Phone No. 202-404-1556
Office of the Associate Counsel
(Patents), Code 1008.2
Naval Research Laboratory
4555 Overlook Ave, SW
Washington, DC 20375-5325

Auto-Reply Facsimile Transmission

TO: Fax Sender at 202 404 7380

Fax Information
Date Received: 5/18/2005 9:44:39 AM [Eastern Daylight Time]
Total Pages: 2 (including cover page)

ADVISORY: This is an automatically generated return receipt confirmation of the facsimile transmission received by the Office. Please check to make sure that the number of pages listed as received in Total Pages above matches what was intended to be sent. Applicants are advised to retain this receipt in the unlikely event that proof of this facsimile transmission is necessary. Applicants are also advised to use the certificate of facsimile transmission procedures set forth in 37 CFR 1.8(a) and (b), 37 CFR 1.6(f). Trademark Applicants, also see the Trademark Manual of Examining Procedure (TMEP) section 306 et seq.

Received Cover Page ========>

05/18/05 WED 09:47 FAX 202 404 7380 NRL CODE 1008.2 PATENTS 001

Fax transmission from:
U.S. Naval Research Laboratory
Associate Counsel Intellectual Property, Code 1008.2
4555 Overlook Avenue, SW
Washington, DC 20375-5325

From: Joe Grunkemeyer
Phone: (202) 404-1556
Fax: (202) 404-7380
Date: 05/18/2005

To: Examiner Kenneth S. Kim
Art Unit 2111
Fax: (703) 872-9306
Cover Sheet + 1 Pages

Message:

RE: Patent Application No.: 09/733,786
Filed: 08/20/2001
Inventor: Sandbote
Docket No.: NC 84,832
Notice of Appeal – 1 page

The information contained in this facsimile may be client confidential, and may also be attorney privileged. The information is intended only for the use of the individual or entity to whom it is addressed. If you are not the intended recipient, you are hereby notified that any use, distribution, or copying of this transmission is prohibited. If you have received this facsimile in error, please notify us immediately by telephone for instructions. Thank you.